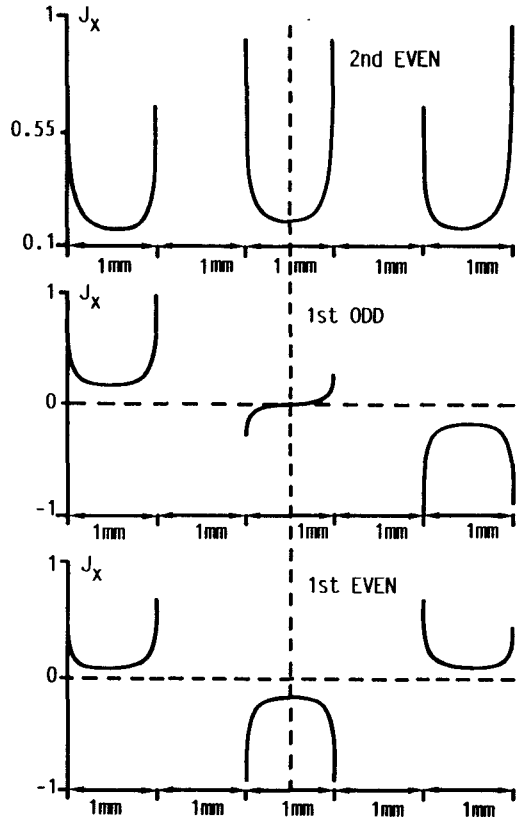

Fig. 9. Longitudinal current J_x at 1 GHz for a three-strip problem with $w_1 = w_2 = w_3 = 1$ mm, $s_{12} = s_{23} = 1$ mm, $d = 1$ mm, and $\epsilon_r = 10$.

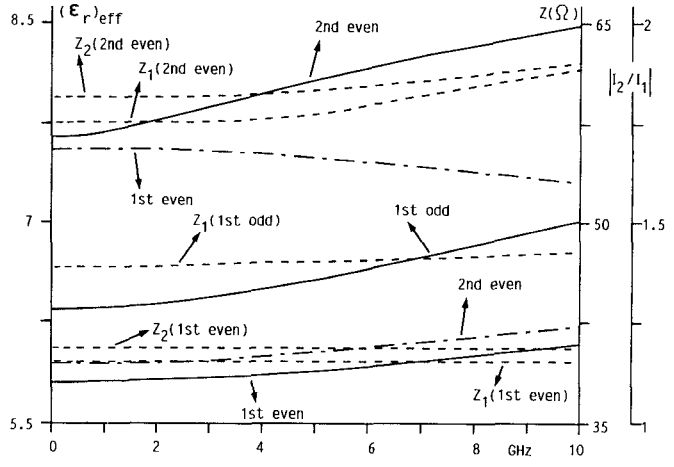

Fig. 10. Dispersion characteristics, power–current impedances, and total longitudinal current ratios for the three-strip configuration of Fig. 9.

For the single-strip configuration we compared the voltage–current, power–voltage, and power–current definitions for the characteristic impedance. It was shown that the power–current definition has the most TEM-like character, as it changes more slowly as a function of frequency than the other definitions. This property also holds good for the double- and triple-strip configurations, as was shown by some typical examples.

By incorporating Meixner's edge conditions and by explicitly satisfying the relevant integral equation in the end points, an accurate solution is ensured for all field quantities in both the low-frequency and the high-frequency range.

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A FET Amplifier in Finline Technique

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***Abstract*—The successful design and realization of a stable FET amplifier in finline technique are presented. The circuit has been realized in integrated E-plane technology and features an input and an output port in unilateral finline and a combined microstrip/coplanar bias circuit. The amplifier has been designed for 17 GHz operation and has a gain of 6 dB over a bandwidth of 1 GHz using a NE67300 FET.**

I. Introduction

In this paper, the design and performance of a novel finline amplifier will be described. The essential features of this amplifier were briefly outlined in [1]. Very little work had been reported previously on the realization of field-effect transistor

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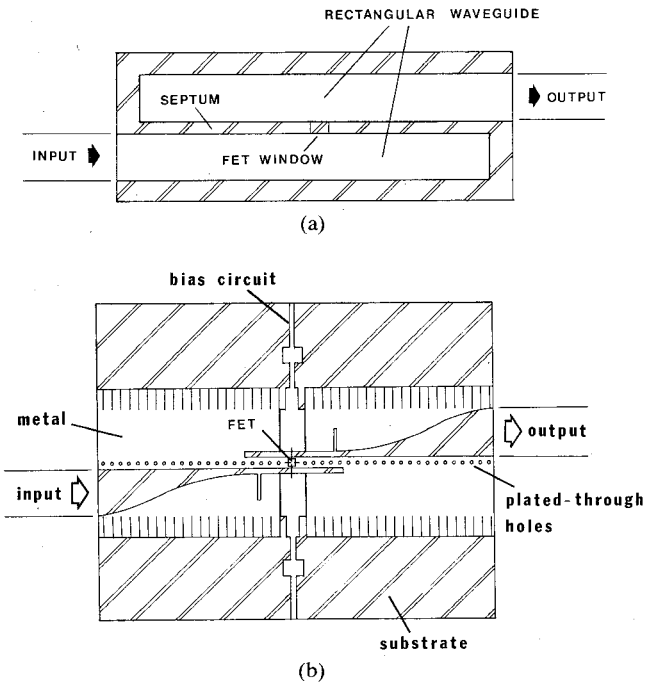

Fig. 1. Basic features of the finline amplifier. (a) Split-block housing. (b) Metallization pattern (schematic).

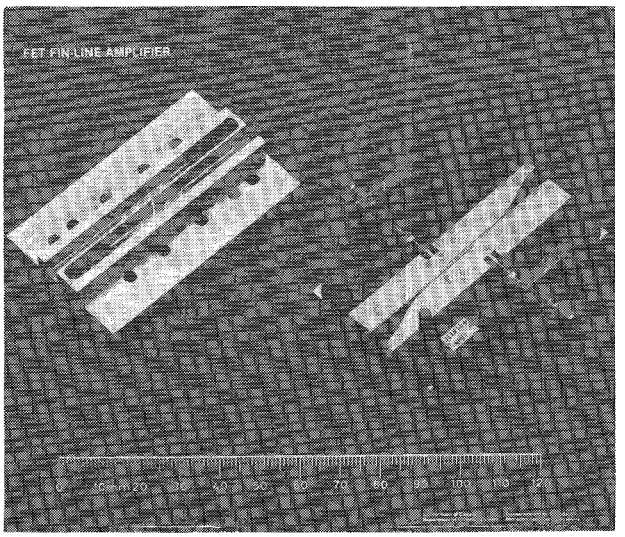

Fig. 2. Photograph of the experimental finline amplifier showing the split-block housing and the planar circuit.

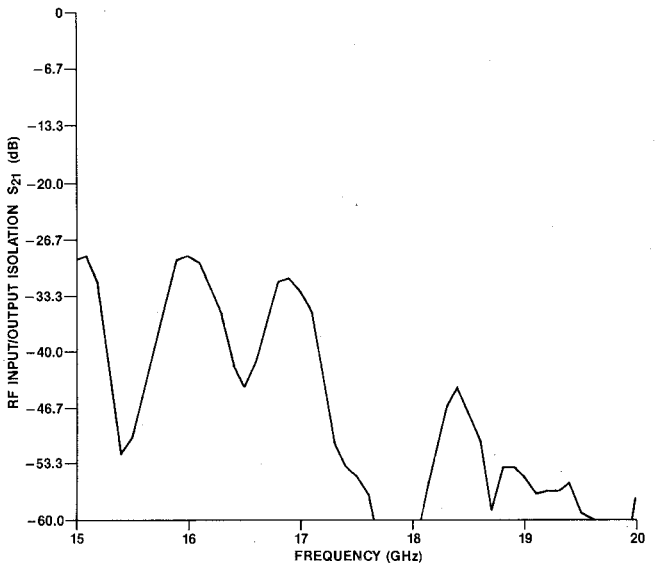

Fig. 3. RF input-to-output isolation of amplifier circuit without transistor.

(FET) amplifiers in finline technology. Indeed, unconditionally stable amplification is difficult to achieve in the finline environment for several reasons. First, the electromagnetic fields extend beyond the immediate vicinity of the finline gap, making impedance matching of FET's and the suppression of undesirable feedback more difficult than in microstrip. Second, the finline, when below cutoff, offers a very large *VSWR* to the device, making it potentially unstable at lower frequencies.

To overcome these difficulties, Ebner *et al.* [2] have placed a FET in a microstrip mount with antipodal finline transitions to the input and output waveguide ports. To stabilize the device at frequencies below cutoff, they have added a dissipative slot in each transition. Even though a very good RF to dc isolation can be achieved in this manner, the addition of absorbing material and of long lossy transitions is detrimental to the performance of such an amplifier, particularly if it is to be integrated into a complete finline subassembly. A similar amplifier at 9.2 GHz has been reported by Derwischew and Senf [3].

Other researchers have mounted FET's in finlines to realize oscillators [4]–[6]. However, in these designs, spurious oscillations due to the cutoff behavior of the finline have not been considered, and the natural feedback provided by the finline environment has been exploited to provide, at least partly, the oscillation condition.

Therefore, none of these circuits is suitable for amplification in their original form. However, by modifying the configuration proposed by Jacob and Ansorge [5], an unconditionally stable finline amplifier has been designed and realized. In the following, this new design will be described, and measurements of its performance will be presented.

II. Description of the Circuit Topology

The RF circuit of the finline amplifier vaguely resembles the oscillator topology proposed by Jacob and Ansorge [5]. However, the input and output finlines run straight and in parallel rather than in a boomerang shape, and are shielded from each other by a thin electric wall or septum. Both lines are unilateral single-fin lines, which have only half the impedance of a regular symmetrical finline. The transistor sits in a narrow opening of the septum and is coupled magnetically to the input and output lines with bond wires, as shown in Fig. 1(a) and (b). A photograph of the printed circuit and its housing is shown in Fig. 2.

In the prototype described in this paper, both ports originate in WR(42) waveguide and are tapered down to a single-fin unilateral finline with a gap width of 0.18 mm, having a power–voltage impedance of 83 Ω and an effective dielectric constant of 1.11 at 16.8 GHz. Bond wires are attached to the gate and drain pads of the transistor and bonded to the metallization across the input and output slots. The source pads of the FET chip are grounded to the central metallization. For maximum magnetic coupling, the finlines are short-circuited about one quarter wavelength beyond the bond wires. Fine matching of the input and output impedances of the FET is achieved by adjusting the length of a shunt tuning slot in each line with silver paint.

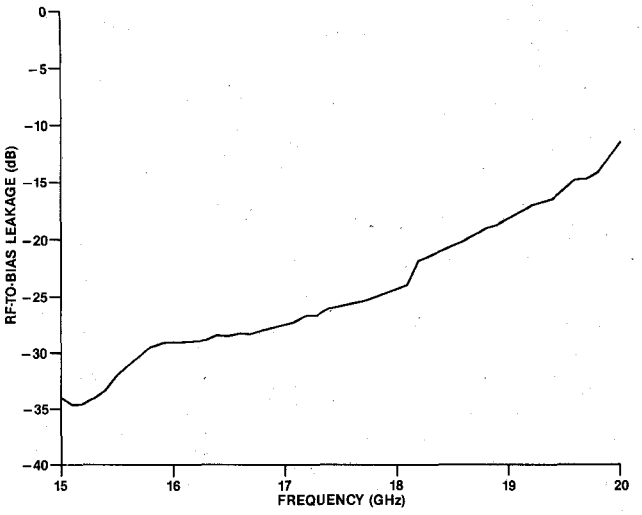

Fig. 4. Leakage from waveguide port to bias port.

The circuit is printed on 0.010-in.-thick RT/Duroid ($\epsilon_r = 2.22$). The metallization is unilateral except for the serrated clamping regions, the microstrip sections, and the central strip containing a series of plated-through holes which extend the shielding septum into the dielectric. The holes have a diameter of 0.35 mm, and their centers are 1 mm apart. Since the spacing between holes is much smaller than the wavelength in the substrate ($\lambda_s = 12$ mm at the design frequency), the parasitic RF coupling between input and output ports (in the absence of the transistor) is less than -30 dB (see Fig. 3).

III. Design of the RF Circuit

The NE 67300 transistor chip was selected for its good performance at the frequency of interest. A standard transistor model was used in the design and analysis of the amplifier. The characteristics of the model were based on the S parameters specified by the manufacturer for frequencies between 2 and 18 GHz in a 50 Ω microstrip environment. The inductance of each pair of bond wires coupling the transistor terminals to the slots was estimated to be 0.5 nH.

The maximum available gain of the NE 67300 is about 10 dB at 17 GHz. The corresponding input and output impedances are very close to the unstable region. To be on the safe side, the amplifier was designed for a gain of only 9 dB. The selected source and load impedances, $Z_s = (10 + j16)$ Ω and $Z_l = (31 + j46)$ Ω, are situated in the safely stable region.

The input and output matching networks contain adjustable elements in the form of short-circuited series stubs. The stubs were dimensioned according to Burton and Hoefer [7] and placed at appropriate distances from the FET. Fine tuning was achieved by adjusting the length of the stubs with silver paint.

IV. Design of the Bias Circuits

Special gate and drain bias circuits were developed to overcome the problem of instability at frequencies below finline cutoff (6 GHz in this case). To achieve this goal, the bias circuits must be invisible to the transistor at RF while presenting a stable load at lower frequencies, where the finline becomes reactive.

The bias circuits begin at the gate and drain bond wires, respectively, as coplanar waveguides, formed by two narrow parallel series slots in the fins (see Fig. 1(b)). These coplanar

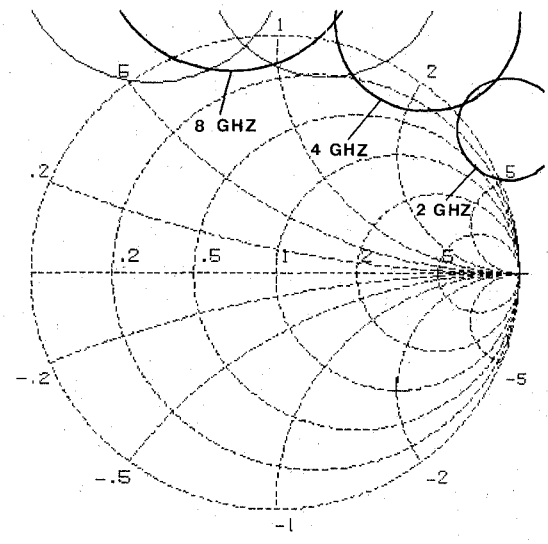

Fig. 5. Stability circles for the NE67300. (a) Input stability circles. (b) Output stability circles.

sections must be half a wavelength long at the center frequency (16.8 GHz), extending from the edge of the fin to the waveguide broad wall. In this manner, the RF short circuit at the wall is transformed into an RF series short at the fin edge. At the design frequency of 16.8 GHz, the physical length of the coplanar sections (7.11 mm) can only be accommodated in the WR(42) waveguide enclosure by running the sections at an angle of about 45° (see Fig. 2). A similar concept was used in the design of finline switches for a QPSK modulator by Gajda and Verver [8]. At the outer broad wall, the coplanar section is transformed into a microstrip line terminated in a 50 Ω load via a bias tee. A microstrip low-pass filter further reduces RF leakage into the bias circuit.

Since the bias circuit is composed of microstrip and coplanar waveguide, a low (50 Ω) impedance can easily be presented to the FET terminals at all frequencies from dc to the cutoff of the filter, thus keeping the transistor stable in this range.

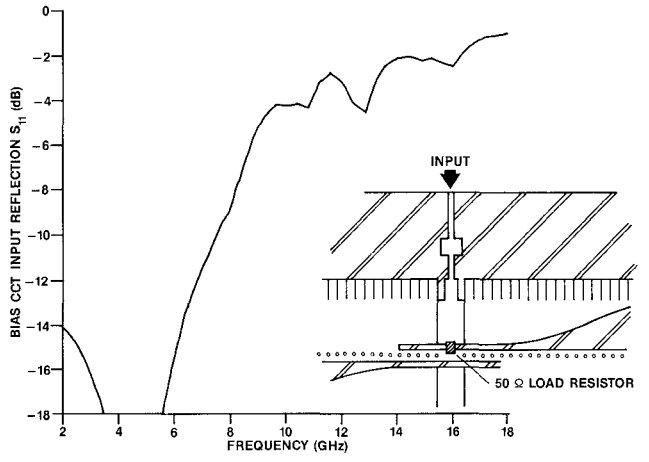

Fig. 6. Input reflection coefficient of the bias circuit measured at the coaxial bias port when the transistor is replaced with a 50 Ω chip resistor.

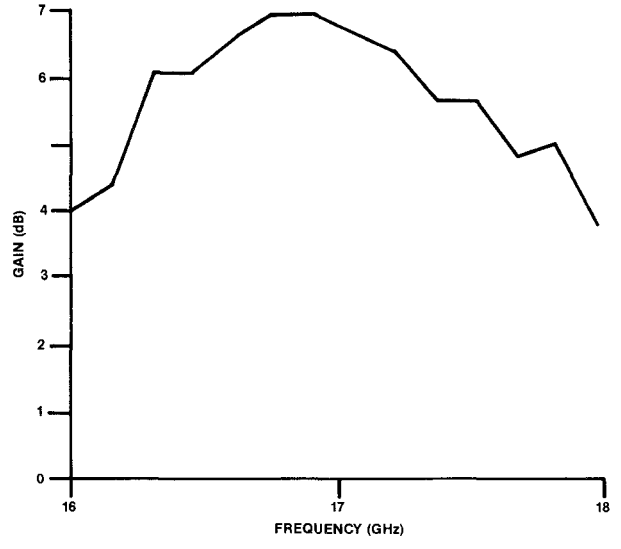

Fig 7. Measured gain of the finline amplifier.

The level of leakage at the operating frequency of the amplifier was measured at about −27 dB, which is quite reasonable. A plot of measured RF leakage from one of the waveguide ports to the coaxial bias connector is shown in Fig. 4.

It is important to consider every potentially unstable region of the device. For the NE67300 FET the most critical and potentially unstable region is in the neighborhood of 4 to 5 GHz, as shown in Fig. 5. To keep the transistor from oscillating, the bias circuit was designed to have a low *VSWR* in that particular frequency region.

The performance of the bias circuits was verified by replacing the transistor with a 50 Ω chip resistor and measuring the reflection coefficient at the microstrip bias input port. The return loss was better than required for all frequencies, especially from 3.5 to 5.6 GHz, where S_{11} was less than −18 dB (see Fig. 6).

V. Amplifier Performance

Tuning of the stubs was performed while measuring the amplifier response. They were accessible through an opening in the sidewall of the housing, situated above the transistor. Once the amplifier was tuned, the opening was closed with a brass cover. Since most of the field energy is concentrated in and around the slot of the finline, the opening had no significant effect on the response of the circuit, and tuning was performed easily.

Before tuning, the circuit had a gain of only about 4 dB at the design frequency. This was probably due to the fact that the influence of the plated-through holes on the finline impedance had not been considered. After tuning, the amplifier was unconditionally stable at all frequencies, and the gain was greater than 6 dB over a 1 GHz bandwidth centered at 16.8 GHz (see Fig. 7). The noise figure was 3.5 dB at that frequency. Failure to achieve the desired gain of 9 dB is due to several factors which were not considered during the design: losses in the input and output networks, tolerances in the device parameters, and differences in the circuit environment. *S* parameters were given for operation in a 50 Ω microstrip but were applied to a finline mount.

VI. Conclusion

A novel FET amplifier concept has been demonstrated by the successful realization of a finline amplifier for 17 GHz. In contrast to previously published solutions, the transistor chip is directly embedded in the finline environment and thus does not require a microstrip environment for RF matching.

An original approach is used to overcome instability problems with FET's in finline structure. Stabilization is achieved by using a unique coplanar/microstrip bias circuit, while RF performance is maintained by decoupling the input and output finlines using plated-through holes. The result is an amplifier with unconditional stability having 6 dB gain and a 3.5 dB noise figure over a 1 GHz bandwidth at 17 GHz. The good performance of the component has encouraged further efforts in this area. In particular, a 18.75/37.5 GHz finline multiplier in this technology is presently under development. Also, the biasing circuit may be implemented in components such as FET oscillators, mixers, and modulators.

Acknowledgment

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